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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,377	04/16/2004	Hiroyuki Yoshida	119331	8390

25944 7590 11/29/2005

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EXAMINER	
TERESINSKI, JOHN	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/825,377	YOSHIDA ET AL.	
	Examiner	Art Unit	
	John Teresinski	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7* is/are rejected.

7)☒ Claim(s) *6,8 and 9* is/are objected to.

8)☒ Claim(s) *10-13* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/16/04, 8/23/04, 6/16/05, 7/28/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figure 1 as indicated in the Description of the Related Art, should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,657,269 to Migliorato et al. in view of U.S. Patent No. 6,411,727 to Harkin.

Regarding claim 1, Migliorato et al. disclose a capacitive sensor cell having M individual power supply lines and N individual output lines, arranged in a matrix of M rows by N columns (column 6 lines 29-31), and electrostatic capacitance detection elements provided on crossing points of the individual power supply lines and the individual output lines (column 6 lines 41-

52), each of the electrostatic capacitance detection elements being formed of a signal detection element, the signal detection element being formed of a capacitance detecting electrode, a capacitance detecting dielectric layer and a reference capacitor, the reference capacitor being formed of a reference capacitor first electrode, a reference capacitor dielectric layer and a reference capacitor second electrode (column 6 lines 30-35, 46-52, Fig. 1 elements C_s, C_r), and the signal amplification element being formed of a MIS type thin film semiconductor device/thin film transistors for signal amplification, including a gate electrode, a gate insulating layer and a semiconductor layer (column 8 lines 1-9, Fig. 1 element 20).

Migliorato et al. disclose a signal amplification element as cited above but fails to teach each of the electrostatic capacitance detection elements being formed of a signal detection element and a signal amplification element. Harkin discloses a fingerprint sensing device and method having an array of capacitive type sense elements (12) including each of the electrostatic capacitance detection elements being formed of a signal detection element and a signal amplification element (column 5 lines 25-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a signal amplification element with each signal detection element as taught by Harkin into Migliorato et al. for the purpose of increased sampling time which provides fast read-out and also much superior noise rejection because of the shorter integration period (column 8 lines 46-58).

Regarding claim 2, Migliorato et al. disclose a drain region of the MIS type thin film semiconductor device for signal amplification being electrically coupled to the individual power supply lines and the reference capacitor first electrode, and a gate electrode of the MIS type thin

film semiconductor device for signal amplification being coupled to the capacitance detecting electrode and the reference capacitor second electrode (column 7 lines 35-44).

Regarding claim 3, Migliorato et al. disclose the reference capacitor dielectric layer and the gate insulating layer of the MIS type thin film semiconductor device for signal amplification being formed with a same material on a same layer (column 9 lines 39-55).

Regarding claims 4 and 5, Migliorato et al. disclose the reference capacitor first electrode and a drain region of the semiconductor film being formed with a same material on a same layer and, the reference capacitor second electrode and the gate electrode being formed with a same material on a same layer (Fig. 3).

Regarding claim 7, Migliorato et al. disclose the capacitance detecting dielectric layer being located on an uppermost surface of the electrostatic capacitance detection device (Fig. 1 and 10, elements 10 and Cs).

Allowable Subject Matter

Claims 6, 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-13 are allowed.

The following is an examiner's statement of reasons for allowance:

Regarding claim10:

The primary reason for the allowance of claim 10 is the inclusion of the signal amplification element being formed of a MIS type thin film semiconductor device for signal

amplification, including a gate electrode, a gate insulating layer and a semiconductor layer; and a part of a drain region and a part of a gate region of the MIS type thin film semiconductor device for signal amplification forming an overlapped portion via the gate insulating layer, and an overlapped portion forms the reference capacitor. It is these features found in the claim, as they are claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this claim allowable over the prior art.

Claims 11-13 are allowed due to their dependency on claim 10.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Teresinski whose telephone number is (571) 272-2235. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diane Lee can be reached on (571) 272-2399. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JT

JT
November 25, 2005

ANJAN DEB
PRIMARY EXAMINER